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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/347,690	07/02/1999	MANPREET S. KHAIRA	884.107US1	4194

7590

07/29/2003

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EXAMINER

CRAIG, DWIN M

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Introduction

1. **Claims 1-28 of U. S. Application 09/347690**, filed on 07/02/1999 are presented for examination. Applicants have entered into the record (although it is noted that the Declaration has not been signed by all of the inventors), *Declaration Under 37 C.F.R. § 1.132, to establish the inapplicability of using the reference authored by Casas et al. "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding of VLSI Design Jan. 7-10, 1999*, including an embedded reference to Khaira et al., "Logic Verification Using Shark", Intel Design and Test Technology Conference, 1997, pp. 259-264, July 1997 to reject the claims under 35 U.S.C. 102(b), (*see Paper #8 5-2-203*), for the Examiner's attention. Please note in response, the following Requirement for Information under 37 C.F.R. 1.105.

Requirement for Information - 37 C.F.R. § 1.105

2. **Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application:**

- Khaira et al., "Logic Verification Using Shark", Intel Design and Test Technology Conference, 1997, pp. 259-264, July 1997.
- The date of the "Intel Invention Disclosure".

3. The non-patent literature, was relied upon by Applicants, as indicated in "*Declaration Under 37 C.F.R. § 1.132, to establish the inapplicability of using the reference authored by Casas et al. "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding of VLSI Design Jan. 7-10, 1999, including an embedded reference to Khaira et al., "Logic Verification Using Shark", Intel Design and Test Technology Conference, 1997, pp. 259-264, July 1997 to reject the claims under 35 U.S.C. 102(b), (see Paper #8 5-2-203), The invention appears to have been in use at Intel and thus constitutes prior art, [see "Intel Invention Disclosure" where it is noted that Applicant's have redacted the dates]*, this art is very relevant to examination of the instant invention and claims, and therefore the applicant should provide the office with copies of the references so that they may further be evaluated for relevance.

4. **The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement.** This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.

Art Unit: 2123

5. The applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained will be accepted as a complete reply to the requirement for that item. Applicants are reminded that they have referred to the material in their response, as evidenced by *Declaration Under 37 C.F.R. § 1.132, to establish the inapplicability of using the reference authored by Casas et al. "Logic Verification of Very Large Circuits Using Shark", Twelfth International Proceeding of VLSI Design Jan. 7-10, 1999, including an embedded reference to Khaira et al., "Logic Verification Using Shark", Intel Design and Test Technology Conference, 1997, pp. 259-264, July 1997 to reject the claims under 35 U.S.C. 102(b), (see Paper #8 5-2-203).*

6. This requirement is subject to the provisions of 37 CFR 1.134, 1.135 and 1.136 and has a shortened statutory period of 2 months. EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136(a).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwain M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 9:00 - 5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
July 20, 2003


KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER